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DESIGN AND PERFORMANCE OF CMOS MICROMECHANICAL RESONATOR OSCILLATORS

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Abstract

A completely monolithic high-Q oscillator, fabricated via a combined CMOS plus surface micromachining technology, is described, for which the oscillation frequency is controlled by a polysilicon micromechanical resonator to achieve high stability. It is shown that the closed-loop, steady-state oscillation amplitude of this oscillator can be controlled through the dc-bias voltage applied to the capacitively driven and sensed μresonator. Brownian motion and mass loading phenomena are shown to have a greater influence on short-term stability in this micro-scale.

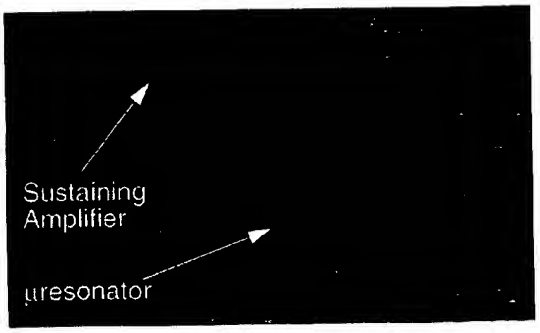

Fig. 1: SEM of the integrated CMOS μresonator oscillator.

Introduction

Crystal oscillators are widely used to generate precision frequency standards for complex integrated circuits. With the current trend to include increasing amounts of a total system on a single silicon chip, designers have begun to include the oscillator function, without the crystal, on the silicon die. A fully monolithic high-Q oscillator, which includes the "crystal" element as well as sustaining CMOS electronics on-chip, is thus desirable.

Such an oscillator has recently been demonstrated [1], which utilizes a surface-micromachined, polycrystalline silicon resonator [2] frequency-setting element and CMOS electronics to sustain oscillation, all fabricated onto a single silicon chip (Fig. 1). The cross-section of the combined CMOS plus surface micromachining technology used to fabricate this oscillator [1,3] is shown in Fig. 2.

With Q's of over 80,000 [4] under vacuum and center frequency temperature coefficients in the range of -10 ppm/°C (several times less with nulling techniques) [5], polysilicon micromechanical resonators can serve reasonably well as miniaturized substitutes for crystals in a variety of high-Q oscillator and filtering applications. As the high-Q element is miniaturized, however, such phenomena as Brownian motion and mass loading noise [6] begin to have greater influence on oscillator short-term stability and may limit the ultimate stability of micro-scale resonators unless design strategies which minimize these effects are implemented. After an initial focus on resonator transducer and oscillator design, this paper will address some of these performance limiting effects.

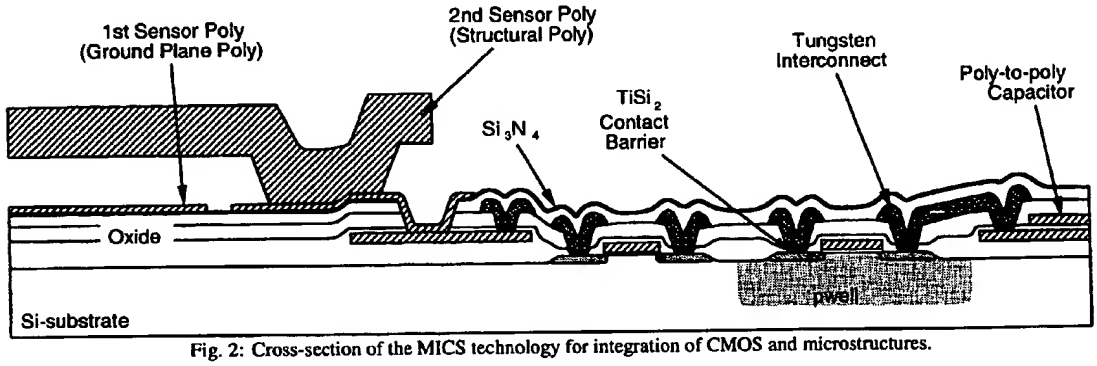

Fig. 2: Cross-section of the MICS technology for integration of CMOS and microstructures.

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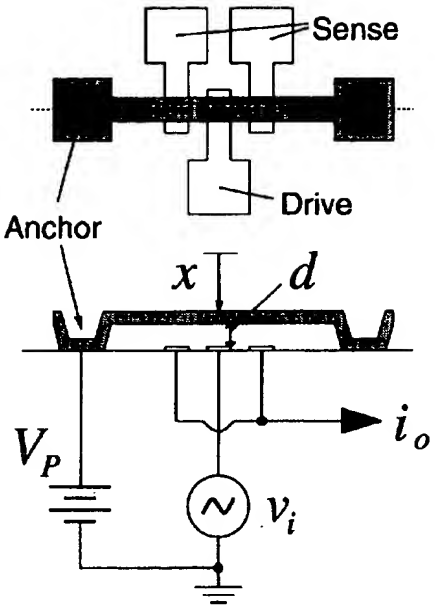


Fig. 3: Overhead and cross-sectional view of a vertical parallel-plate capacitively driven resonator with typical applied bias and excitation voltages.

Resonator Design

To simplify the task of integrating CMOS with micromechanics, capacitive excitation and detection is utilized for the μresonators in this work. A variety of capacitive topologies are available in this technology, and each will dictate the frequency tuning range and stability of the μresonator.

Figure 3 shows the cross-section of a parallel-plate capacitively driven μcantilever resonator in a typical bias and excitation configuration. [7]. Here, an ac voltage v_i electrostatically drives the cantilever. The dc-bias voltage V_P amplifies the resulting force components at the frequency of v_i. In this scheme, the beam-to-electrode capacitance is nonlinearly dependent upon beam displacement, and thus, the change in capacitance vs. displacement, $\partial C/\partial x$, is a strong function of displacement:

$$\frac{\partial C}{\partial x} = \frac{C_o}{d}\left(1-\frac{x}{d}\right)^2 , \qquad (1)$$

where C_o is the static beam-to-electrode capacitance. Using (1), the components of force f_d at the input frequency acting on the beam of Fig. 3 are

$$f_d|_{\omega_o} = \frac{1}{2}(V_P - v_i)^2 \frac{\partial C}{\partial x}\bigg|_{\omega_o} = -V_P\frac{C_o}{d}v_i + V_P^2\frac{C_o}{d^2}x . \qquad (2)$$

The second term of (2) implies an electrical spring constant, $k_e=V_P^2(C_o/d^2)$, which adds to the mechanical spring constant k_m and makes the center frequency f_o a function of the dc-bias voltage V_P:

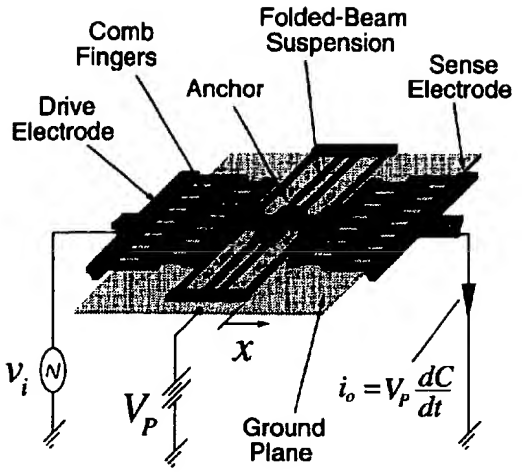


Fig. 4: Perspective view of a two-port, folded-beam, lateral comb-driven resonator with typical applied bias and excitation voltages. All areas of the resonator and electrodes are suspended 2 μm above the substrate, except for the darkly shaded areas, which are the anchor points.

$$f_o = f_o\left(1-\frac{V_P^2 C_o}{k_m d^2}\right)^{1/2} . \qquad (3)$$

The above provides a convenient means for voltage control of the center frequency, making parallel-plate driven resonators useful for VCO applications. A -3600 ppm/V fractional frequency change is typical for a 20 kHz μresonator with a nominal V_P=10 V. However, (3) also suggests that oscillators referenced to parallel-plate capacitively driven μresonators are less stable against power supply variations, due to electronic noise or temperature. If V_P=10 V is supplied by a Zener diode reference, which typically varies 250 mV over a 0°-100°C range, the corresponding fractional frequency variation for a 20 kHz μresonator is 864 ppm over this temperature range. If a bandgap reference is used (3 mV variation over a 0°-100°C range), the $\Delta f/f_o$ variation is 10 ppm.

To eliminate this component of frequency instability, the electrode-to-resonator capacitance must be made to vary linearly with resonator displacement. In this work, this is achieved by using interdigitated-comb finger drive and sense capacitors [2]. Figure 4 shows a μresonator which utilizes interdigitated-comb finger transduction in a typical bias and excitation configuration. The μresonator consists of a shuttle mass, with fingers on opposite sides, suspended 2 μm above the substrate by folded flexures, which are anchored to the substrate at two central points. The shuttle mass is free to move in the direction indicated, parallel to the plane of the silicon substrate. Folding the suspending beams as shown provides two main advantages: first, post-

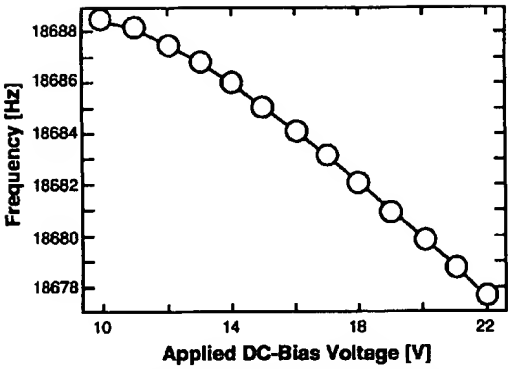


Fig. 5: Plot of center frequency vs. dc-bias voltage V_P for a comb-driven μresonator.

fabrication residual stress is relieved if all beams expand or contract by the same amount; and second, spring stiffening nonlinearity in the suspension is reduced, since the folding truss is free to move in a direction perpendicular to the resonator motion.

The drive and sense capacitors consist of overlap capacitance between the interdigitated shuttle and electrode fingers. As the shuttle moves, these capacitors vary linearly with displacement. Thus, $\partial C/\partial x$ is a constant, making the drive force f_d at the input frequency independent of x:

$$f_d|_{\omega_o} = V_P \frac{\partial C}{\partial x} v_i . \qquad (4)$$

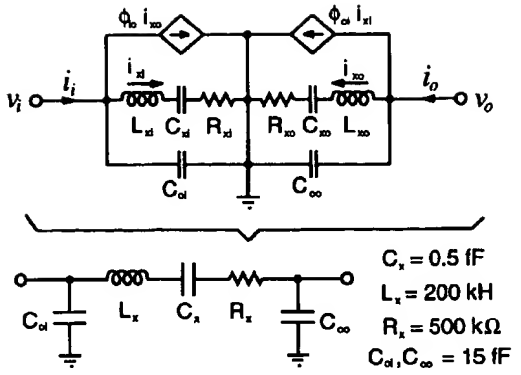
The electrical spring constant k_e is, thus, ideally nonexistent, and the resonator center frequency is independent of V_P.

For actual comb-driven μresonators, nonidealities do not permit absolute cancellation of k_e, and some variation of frequency with V_P is observed. Figure 5 shows a plot of center frequency vs. dc-bias for a micromachined comb-driven resonator. The frequency variation is about -54 ppm/V, corresponding to 14 ppm and 0.2 ppm fractional frequency variations over a 0°-100°C range for a Zener diode and a bandgap reference, respectively.

Oscillator Design

The equivalent circuit for the two-port μmechanical resonator of Fig. 4, shown transformed to an equivalent LCR representation, is presented in Fig. 6 [7,8]. Due to the use of weak capacitive electromechanical transduction, the motional element values are quite different from those for quartz crystal units (which typically have R_x=50Ω, C_x=0.04 pF, L_x=0.25 H), and this dictates differing strategies in the design of μresonator oscillators versus macroscopic crystal oscillators. The detailed, transistor-level circuit design and operation of this oscillator has already been discussed elsewhere [1]. The focus of the present discussion centers on issues of amplitude limiting.

Figure 7 shows a system-level schematic describing the basic architecture used for this oscillator. Since the



$$R_{xn} = \sqrt{km}\left[QV_P^2(\partial C/\partial x)_n^2\right]^{-1} \qquad C_{xn} = k^{-1}V_P^2(\partial C/\partial x)_n^2$$

$$L_{xn} = m\left[V_P^2(\partial C/\partial x)_n^2\right]^{-1} \qquad \phi_{mn} = \frac{(\partial C/\partial x)_m}{(\partial C/\partial x)_n}$$

Fig. 6: Equivalent circuit for a two-port μresonator showing the transformation to the more convenient LCR form. In the equations, k is the system spring constant and $(\partial C/\partial x)_n$ is the change in capacitance per displacement at port n of the μresonator.

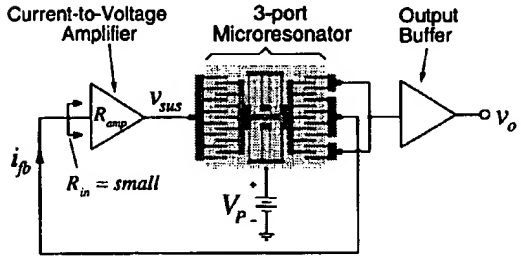


Fig. 7: System level schematic for the μresonator oscillator.

motional resistance of the μresonator is large (Fig. 6), a series resonant oscillator architecture is utilized to minimize Q-loading [1]. As shown, the system consists of a three-port micromechanical resonator, for which two ports are embedded in a positive feedback loop with a sustaining transresistance amplifier, while a third port is directed to an output buffer. The use of a third port effectively isolates the sustaining feedback loop from variations in output loading. Conceptually, the sustaining amplifier and μmechanical resonator comprise negative and positive resistances, respectively. During start-up, the negative resistance of the amplifier R_{amp} is larger in magnitude than the positive resistance of the resonator R_x, and oscillation results. Oscillation builds up until either some form of nonlinearity or a designed automatic-level control circuit alters either or both resistors so that, R_{amp}=R_x, at which point the oscillation amplitude limits.

For oscillators controlled by quartz crystals, the nonlinearity usually appears in the sustaining circuit, where transistors enter the triode region at large voltage amplitudes,

reducing effective device transconductances until the loop gain drops to unity. Limiting due to crystal nonlinearity is rare, since quartz crystal units display very little nonlinearity over normal oscillator operating voltage ranges [9].

On the other hand, even though comb-driven, folded-beam μmechanical resonators are only slightly less linear than crystals [1], limiting due to nonlinearity in flexural-mode μresonators is quite practical through adjustment of the dc-bias voltage V_P. As seen from the equations of Fig. 6, the values of the motional circuit elements representing the capacitively driven μmechanical resonator are strongly dependent upon the dc-bias voltage V_P applied to the resonator. In particular, the value of motional resistance R_x is inversely proportional to the square of V_P, and thus, it can be set to just under R_{amp} at the start of oscillation by proper selection of V_P. As oscillation builds up, stiffening nonlinearities in the resonator springs then increase the effective R_x of the μresonator until R_x=R_{amp}, when the loop gain equals one and the amplitude limits. The steady-state amplitude of oscillation is thus a function of the initial separation between R_x and R_{amp}, which is in turn a function of V_P.

To quantify this limiting process, we first write an expression describing the spring nonlinearity. Since at resonance, the force is amplified by the Q, we have

$$Qf = k_1 x + k_2 x^2 + k_3 x^3 + \ldots, \tag{5}$$

where k_1 is the small displacement system spring constant, and k_2 and k_3 model the spring nonlinearity. A series reversion then yields

$$x = b_1 Qf + b_2 (Qf)^2 + b_3 (Qf)^3 + \ldots, \tag{6}$$

where $b_1 = k_1^{-1}$, $b_2 = -k_2 k_1^{-3}$, and $b_3 = 2k_2^2 k_1^{-5} - k_3 k_1^{-4}$. Retaining only those components at resonance, the phasor form for displacement X is then given by

$$X = b_1 QF + \frac{3}{4} b_3 Q^3 F^3. \tag{7}$$

Inserting expressions for current I_x as a function of X and force F in terms of input voltage V_i into (7) [8], assuming a Duffing nonlinearity in the resonator springs (k_2=0), and differentiating, we have

$$\frac{\partial I_x}{\partial V_i} = \frac{Q}{k_1}\omega_o V_P^2\left(\frac{\partial C}{\partial x}\right)^2 - \frac{9}{4}\frac{k_3 Q^3}{k_1^4}\omega_o V_P^4\left(\frac{\partial C}{\partial x}\right)^4 V_i^2 = \frac{1}{R_{ss}} \tag{8}$$

Equation (8) shows that as the amplitude of oscillation V_i grows, the small-signal series resistance R_{ss} increases until it equals the transresistance of the sustaining amplifier, R_{amp}, at which point the loop gain is unity, and V_i settles at a steady-state value. From (8), the steady-state V_i is clearly controllable through the resonator dc-bias voltage V_P.

Fabrication

The enabling technology for the fully monolithic high-Q oscillator combines planar CMOS processing with surface micromachining [3]. The technologies are combined in a modular fashion, in which the CMOS processing and surface micromachining are done in separate process modules, with no intermixing of CMOS or micromachining steps. This Modular Integration of CMOS and microStructures (MICS) process has the advantage in that it allows the use of nearly any CMOS process with a variety of surface micromachining processes.

In order to avoid problems with microstructure topography, which commonly includes step heights of 2 to 3 μm, the CMOS module is fabricated before the microstructure module. Although this solves topography problems, it introduces constraints on the CMOS. Specifically, the metallization and contacts for the electronics must be able to survive post-CMOS micromachining processing with temperatures up to 835°C. Aluminum interconnect, the industry standard, cannot survive these temperatures. For this reason, tungsten with $TiSi_2$ contact barriers is used as interconnect for this process.

A cross-sectional outline of the MICS process sequence is presented in Fig. 8. The fabrication process begins with standard CMOS up to and including the contact cut for the first metallization (Fig. 8(a)). At this point, a thin film of titanium is sputter deposited onto the wafer surface, and then rapid-thermal annealed (RTA) for 30 seconds at 600°C in a nitrogen ambient to form $TiSi_2$ at points where titanium contacts silicon. Unreacted titanium is then etched away using a 3:1 NH_4OH:H_2O_2 solution, and another RTA is performed for 10 seconds at 1000°C. At this point, the cross-section appears as in Fig. 8(b). A 6000 Å film of tungsten is then sputter deposited and patterned to form the single-level interconnect (Fig. 8(c)). Subsequent low-pressure chemical vapor depositions (LPCVD) of 5000 Å of low-temperature oxide (LTO) and 1500 Å of silicon-rich nitride, at 450°C and 835°C, respectively, serve to passivate the metal (Fig. 8(d)).

Vias are then plasma etched through the nitride and underlying oxide to expose gate polysilicon runners that were formed during CMOS processing (Fig. 8(e)). These runners serve as an intermediate conductive level that joins the CMOS tungsten interconnect with the structural polysilicon interconnect. Direct contact between the first structural (ground plane) polysilicon and tungsten metal never occurs. This originally was a precaution to prevent contamination of the polysilicon deposition system by tungsten.

Next, 3000 Å of *in situ* phosphorous-doped LPCVD polysilicon is deposited at 610°C and patterned to define the interconnect and ground plane polysilicon for the microstructures (Fig. 8(f)). This is followed by a 2 μm LPCVD deposition (450°C) of phosphosilicate glass (PSG) that serves as a sacrificial layer to be removed when releasing the mechanical structures. Next, a contact cut in the PSG defines the anchor points for resonators and electrodes (Fig. 8(g)), and 2 μm of *in situ* phosphorous-doped LPCVD

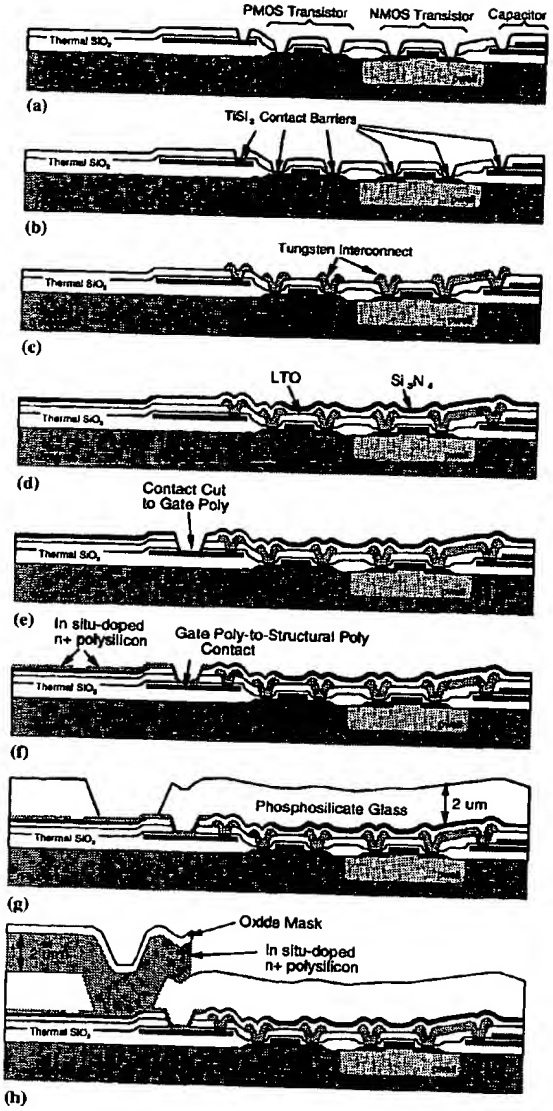


Fig. 8: Cross-sectional process flow for the CMOS plus microstructures fabrication technology. (a)-(c) constitute the metallization steps; (d)-(f) present the circuit-to-structure interface; and (g)-(h) show the micromachining steps. The final cross-section is presented Fig. 1.

polysilicon is deposited at 610°C to serve as the structural material.

The structural material is then capped with a 5000 Å film of LTO, which deposits conformally onto the polysilicon. A thin layer of photoresist is applied and patterned with a single mask that defines resonator geometries, including

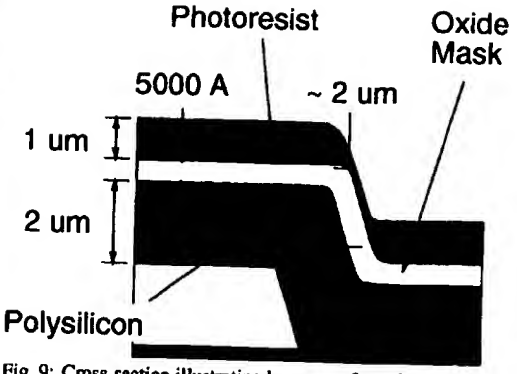


Fig. 9: Cross-section illustrating how a conformal oxide mask can reduce photoresist thickness requirements over large steps, thus, enhancing lithographic resolution. The oxide is much thicker vertically in the regions where photoresist is thin.

interdigitated-comb fingers. The oxide cap is first plasma etched using a CF_4/C_2F_6-based chemistry, which is very selective towards oxide, but which etches silicon very slowly. The oxide then serves as a hard mask for the ensuing plasma etch that patterns the structural polysilicon. This etch is done using a Cl_2-based chemistry that attacks silicon, but etches oxide very slowly. At this point, the structural polysilicon is fully patterned, and the cross-section of Fig. 8(h) results.

Use of this oxide mask greatly enhances the resolution with which finger gaps may be defined. Without the oxide mask, a double or triple layer of photoresist would be required to insure proper coverage of large steps, which occur around the anchors of the resonators and electrodes. With an oxide mask, however, the photoresist is no longer required to cover large steps, since now oxide protects the underlying polysilicon. During the oxide mask etch, the oxide along the step slopes may be attacked, since the photoresist is very thin along the steep slopes. However, as illustrated in Fig. 9, the vertical thickness of the conformal oxide layer is much larger along the these slopes, so oxide will remain to protect polysilicon even after long anisotropic overetches during oxide mask patterning. Thus, a much thinner film of photoresist may be used when an oxide mask is present, which leads to improved lithographic resolution. High resolution is extremely important for oscillator or signal processing applications of capacitively transduced resonators, since the degree of electromechanical coupling achievable via capacitive transduction is directly related to the gap spacings between interdigitated fingers.

Continuing with the process flow, a stress anneal is performed via RTA for 1 minute at 950°C, followed by a sequence of etches to expose the conductive backside of the silicon wafer. Finally, the wafer is dipped in 5:1 buffered hydrofluoric acid to remove the sacrificial PSG and free the microstructures. The wafers are dried using a supercritical carbon dioxide technique, which prevents sticking of the

structures to the substrate by eliminating surface tension forces during drying [13]. The final cross-section is shown in Fig. 1.

Although quite different from the traditional 1 hour at 1050°C furnace stress anneal [2], which cannot be used here due to the presence of CMOS electronics, the rapid thermal stress anneal performs comparably. However, due to the heavy phosphorous concentration in the polycrystalline silicon, the residual compressive stress in the polysilicon films of this work is still quite large and is difficult to anneal away. Thus, stress-relaxing designs, such as cantilevers or folded-beam resonators, are required for the current process. The aforementioned stress problems may be alleviated in the future by lowering the phosphorous content in the μresonators, or by using *in situ* boron-doped polysilicon. The latter solution has the additional advantage of substantially reducing the polysilicon deposition rate.

Short-term Frequency Stability

Superposed Electronic Noise

The phase noise power due to superposed electronic noise from the sustaining amplifier may be predicted theoretically using a procedure similar to that in [10]. Assuming a linear oscillator, and thus, neglecting $1/f$ mixed noise, the equation for the relative oscillator phase noise density N_{op} to carrier C power ratio at a deviation f_m from carrier frequency f_o is

$$\left.\frac{N_{op}}{C}\right|_{\delta f = f_m} = \frac{\left(\bar{i}_a^2/\Delta f\right)R_{amp}^2}{R_L R_{in} C}\frac{1}{8Q^2}\left(\frac{f_o}{f_m}\right)^2. \qquad (9)$$

where R_{in} and R_L are the input and load resistances, respectively.

For the case of an oscillator utilizing a micro-scale resonator, the noise current power $\bar{i}_a^2$ above must include both contributions from the amplifier and from Brownian motion of the miniaturized resonator. Using the thermal equilibrium arguments of [11], the Brownian noise displacement at resonance is given by

$$\frac{\bar{x}_n^2}{\Delta f} = \frac{4Q\sqrt{m}k_B T}{k^{3/2}} \propto \sqrt{m}\,, \qquad (10)$$

where k is the (small displacement) spring constant, k_B is the Boltzmann constant, and T is temperature. Equation (10) predicts that as a resonator is further miniaturized, the noise displacement power due to Brownian motion will decrease, which at first glance would seem to improve noise performance. However, capacitive transduction detects the velocity of the resonator, not its displacement. Thus, the output current i_x of the μresonator corresponds to velocity, and the effective noise current due to Brownian motion is given by

$$\frac{\bar{i}_x^2}{\Delta f} = \frac{4k_B T}{R_x} \propto \frac{1}{\sqrt{m}}\,, \qquad (11)$$

which increases as resonator size decreases. For the oscillator design of this work, the electronic noise contribution from Brownian motion is usually equal to or less than that from the sustaining amplifier.

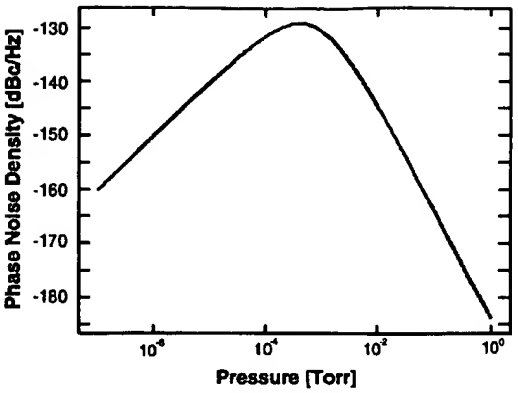


Fig. 10: Predicted plot of mass loading-derived phase noise density 100 Hz off the carrier vs. pressure for a 14.4 kHz μresonator oscillator in an ambient of gas molecules with the molecular weight of nitrogen.

Mass Loading Noise

In addition to superposed electronic noise, any physical phenomenon which causes instantaneous frequency deviations in the resonator will contribute to the total phase noise power. Given that the typical mass of a μmechanical resonator is on the order of 10^{-11} kg, mass loading noise is expected to make a sizable contribution. Mass loading noise [6] arises from instantaneous differences in the rates of adsorption and desorption of contaminant molecules to and from the resonator surface, which cause mass fluctuations, and consequently, frequency fluctuations. Some of the factors which determine the magnitude of mass loading noise include the adsorption/desorption rate of contaminant molecules, contaminant molecule size and weight, pressure, and temperature.

An expression which estimates the phase noise density due to mass loading noise has been proposed by Yong and Vig [6], and is repeated, here:

$$S_\phi(f) = \frac{8r_o r_1 (\Delta f)^2 / N}{(r_o + r_1)^3 + 4\pi^2 f^2 (r_o + r_1)} \cdot \frac{1}{f^2}, \qquad (12)$$

where r_o is the mean rate of arrival of contaminant molecules at a resonator site, r_i is the desorption rate of molecules from the surface, and N is the total number of sites on the resonator surface at which adsorption or desorption can occur. Equation (12) assumes a sticking probability of one if an adsorption site is uncontaminated and zero if contaminated, so the magnitude of phase noise predicted will be higher or lower than the actual value, depending upon the actual sticking probabilities for the molecules involved. The qualitative trends predicted by (12), however, are useful.

Using (12) and accounting for the pressure dependence of r_o [6], the phase noise density due to mass loading for the 14.4 kHz μresonator of Fig. 1 can be plotted as a function of

pressure. Figure 10 presents such a plot for phase noise at a 100 Hz deviation from the carrier, where a contaminant molecule with the molecular weight of nitrogen has been assumed. The desorption energy was assumed to be 12 kcal/mol. The mass loading-derived phase noise density is largest at an intermediate value of pressure and smallest at the higher and lower pressures. At the peak (around 0.5 mTorr), the predicted phase noise density is -130 dBc/Hz, which is higher than that predicted for macroscopic quartz resonators of comparable frequency.

As the μresonator frequency increases, its mass generally decreases, and the phase noise contribution from mass loading is expected to become even more significant. The mass of a 10.7 MHz tuning fork μresonator is on the order of only 10^{-12} kg, and for this design the predicted phase noise density due to mass loading at the peak of the pressure curve is −105 dBc/Hz for 100 Hz deviation from the carrier and −142 dBc/Hz for 5 kHz deviation from the carrier.

For μmechanical resonators with Q's in the range of 50,000 to 500,000, viscous gas damping [12] ceases to be the dominant energy dissipation mechanism at pressures in the range of 0.1 to 1 mTorr, where intrinsic material damping mechanisms become dominant, and the Q of the resonator is maximized. As seen from Fig. 10, the phase noise density due to mass loading may still be large at this pressure value, and even lower pressures are required to alleviate this noise source. Thus, by setting an upper limit on operation pressure given a required phase noise density level, mass loading phenomena may ultimately dictate the design of μmechanical resonator oscillators.

On-chip vacuum encapsulation techniques have been previously investigated which provide vacuums with pressures below 300 mTorr [16], or perhaps better [14,15]. Encapsulation strategies which use gettering elements to remove residual gases may potentially provide the even lower pressure ranges (10^{-7} to 10^{-6} Torr) requested by Fig. 10.

Experimental Results

The fabricated oscillator was bonded up in a dual-in-line package and tested under a variable pressure vacuum probe station. Figure 11 shows a typical oscilloscope plot for a 16.5 kHz version of this oscillator. The amplitude of oscillation was visibly controllable through adjustment of V_P, consistent with the discussion of Section III. A measured plot of steady-state oscillator output voltage versus μresonator dc-bias is presented in Fig. 12. Over most of the range of V_P, the oscillation was visibly and measurably clean. However, over about a 5 V range some chaotic behavior of the resonator was visible under microscope. This indicates that in a finite range of dc-bias voltage, the oscillator may be exhibiting second-order nonautonomous behavior when limiting through resonator nonlinearity [17]. This phenomenon is currently under investigation.

In addition, accurate measurements of the phase noise of this oscillator are in progress.

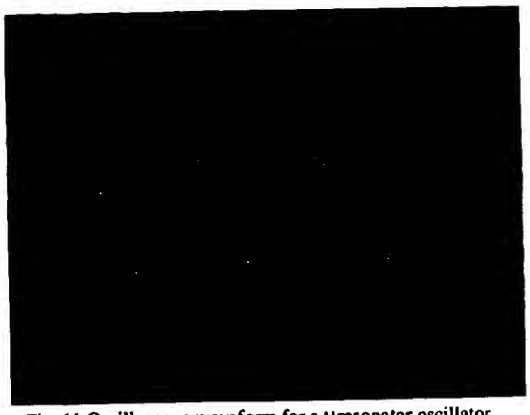


Fig. 11:Oscilloscope waveform for a μresonator oscillator.

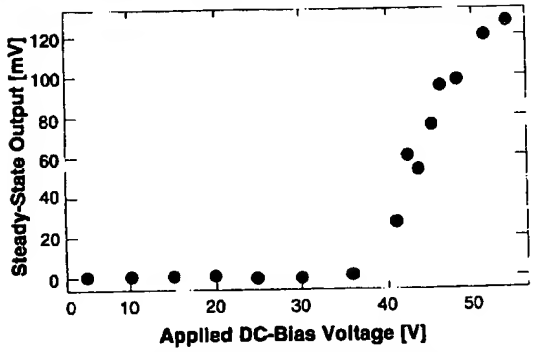


Fig. 12:Measured dependence of oscillator steady-state voltage output amplitude as a function of μresonator dc-bias.

Conclusions

Completely monolithic, highly stable, high-Q oscillators utilizing surface-micromachined polysilicon mechanical resonators have been designed, fabricated, and tested with particular attention to amplitude control and phase noise performance. Due to the novelty of the process and the devices, conservative measures were taken for the designs, and oscillators up to only 100 kHz were fabricated. Designs up to a few megaHertz are feasible using folded-beam resonator designs, and higher frequencies (tens of MHz) should be feasible using more advanced designs aimed at maximizing resonator quality factor, which may otherwise degrade with increasing frequency. Both material and architectural improvements should be possible to increase μresonator Q.

The consequences associated with miniaturization of high-Q elements were addressed via this oscillator. Brownian motion and mass loading were identified as phenomena which become increasingly important contributors to phase noise as resonator dimensions shrink. According to theory, mass loading-induced phase noise can be substantially

reduced by operating the miniature μmechanical resonator under very low pressures. For this reason, integrated vacuum encapsulation techniques may play an important role in the future.

Acknowledgements. The authors would like to thank Shenqing Fang for assistance in CMOS fabrication, as well as Katalin Voros and the staff of the Berkeley Microfabrication Laboratory for process support. In addition, we are grateful for discussions with John Vig of the U.S. Army Electronics Technology and Devices Laboratory, whose insights on mass loading contributed much to this work. This research was supported by the Berkeley Sensor & Actuator Center (BSAC).

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Embedded Micromechanical Devices for the Monolithic Integration of MEMS with CMOS

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Abstract

A flexible, modular manufacturing process for integrating micromechanical and microelectronic devices has been developed. This process embeds the micromechanical devices in an anisotropically etched trench below the surface of the wafer. Prior to microelectronic device fabrication, this trench is refilled with oxide, chemical-mechanically polished, and sealed with a nitride cap in order to embed the micromechanical devices below the surface of the planarized wafer. The feasibility of this technique in a manufacturing environment has been demonstrated by combining a variety of embedded micromechanical structures with a 2 μm CMOS process on 6 inch wafers. A yield of 78% has been achieved on the first devices manufactured using this technique.

Introduction

Recently, a great deal of interest has developed in manufacturing processes that allow the monolithic integration of MicroElectroMechanical Structures (MEMS) with driving, controlling, and signal processing electronics. This integration promises to improve the performance of micromechanical devices as well as the cost of manufacturing, packaging, and instrumenting these devices by combining the micromechanical devices with an electronic sub-system in the same manufacturing and packaging process. For example, Analog Devices has developed and marketed an accelerometer [1] which illustrates the viability and commercial potential of this integration. They accomplished this task by interleaving, combining, and customizing their manufacturing processes which produce the micromechanical devices with the processes that produce the electronics. In another approach, researchers at Berkeley [2] have developed a modular integrated approach in which the aluminum metallization of CMOS is replaced with tungsten to enable the CMOS to withstand subsequent micromechanical processing.

In order to maintain the modularity of the Berkeley approach but overcome some of the manufacturing challenges of their CMOS-first approach, we have developed a MEMS-first process. This process places the micromechanical devices in a shallow trench, planarizes the wafer, and seals the micromechanical devices in the trench. These wafers with the completed, planarized micromechanical devices are then used as starting material for a conventional CMOS process. This technique is equally applicable to other microelectronic device technologies such as bipolar or BiCMOS. At Sandia's Microelectronics Development Laboratory, both 2 μm and 0.5 μm CMOS technologies on 6 inch wafers are available; the 2 μm process is being used as the development vehicle for the integrated technology. Since this integration approach does not modify the CMOS processing flow, the wafers with the subsurface micromechanical devices can also be sent to a foundry for microelectronic processing. Furthermore, the topology of multiple polysilicon layers does not complicate subsequent photolithography. A high-temperature anneal is performed after the devices are embedded in the trench prior to microelectronics processing. This anneal stress-relieves the micromechanical polysilicon and ensures that the subsequent thermal budget of the microelectronic processing does not affect the mechanical properties of the polysilicon structures. This anneal can affect the doping profile of commonly used epitaxial starting material; however, this effect can be easily addressed by increasing the epitaxial layer thickness of the starting material.

Process Description

Figure 1 is a schematic cross-section of the integrated technology. First, alignment marks are etched onto the surface of wafer in order to provide reference locations for subsequent processing. A shallow trench (~ 6 μm for the single-level polysilicon structures described here) is etched in (100) silicon wafers using a KOH etchant. The KOH etchant preferentially etches the (100) crystal plane and produces a trench with sidewalls having a (111) orientation and a slope of 54.7° relative to the surface. This slope aids in the subsequent photo patterning of the MEMS within the wells.

The alignment marks from the top surface of the wafer are used as references to generate another set of

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alignment marks on the bottom surface of the trench. This approach is used to optimize level-to-level registration and resolution of features within the trench. Feature sizes with critical dimensions as small as 1 μm were successfully defined within the trench.

A silicon nitride film is deposited to form a dielectric layer on the bottom of the trench. Sacrificial oxide and multiple layers of polysilicon are then deposited and patterned in a standard surface micromachining process. Polysilicon studs provide contact between the micromechanical devices and the CMOS; the depth of the trench is sized so that the top of the polysilicon stud lies just below the top of the planarized trench. The shallow trenches are then filled with a series of oxide depositions optimized to eliminate void formation in high-aspect-ratio structures. The wafer is subsequently planarized with chemical-mechanical polishing (CMP). The entire structure is annealed to relieve stress in the structural polysilicon and sealed with a silicon nitride cap. At this point, conventional CMOS processing is performed. The backend of the process requires additional masks to open the nitride cap over the micromechanical layer prior to release of the micromechanical structures.

Photoresist is used as a protection layer over the exposed bond pads during the release process. The slow etching of the undoped, densified glasses used as sacrificial layers and the ability of this photoresist to withstand long, HF-based etches is presently a factor that imposes limits on the design rules used for spacing of release access holes in the structure. Development of photopatterning processes with greater resistance to release etches as well as sacrificial layers with greater etch rates is ongoing.

Results

Figure 2 shows a cross-sectional view of an anchor point for the MEMS device within a trench after planarization. The silicon nitride dielectric layer, the ground plane polysilicon, the micromechanical polysilicon and the sacrificial/planarizing layers are easily seen in this Scanning Electron Micrograph (SEM). Figure 3 is a close-up view of the polysilicon interconnects on the bottom of the trench leading to the polysilicon stud that connects to the CMOS metal. This SEM was taken from a wafer removed from the development lot prior to CMOS fabrication. The micromechanical devices were then released and tested to verify the functionality of the micromechanical designs.

Figure 4 shows a portion of a die from the first completed lot. The figure contains surface-micromachined polysilicon resonators in a trench alongside CMOS sensing electronics. Additional devices including CMOS diagnostic structures, MEMS diagnostic structures, combustible gas detectors and accelerometers were also fabricated on this wafer. The layout of the completed die is shown in Figure 5. The completed MEMS structures showed no mechanical degradation with respect to MEMS structures which had not seen the CMOS process. This first wafer was tested at the wafer scale for parametric and functional data. The CMOS parametrics agreed within acceptable process control limits with our unmodified 2 μm CMOS process. Due to tester limitations, only the combustible gas sensors were tested at the wafer level in a fully-coupled CMOS/MEMS mode. These devices showed a yield of 78% as shown in the wafer map of Figure 6. The combustible gas sensor control circuitry included an op-amp and a set of power MOSFETs. The functional yield data on the control circuitry for the accelerometers and resonators was similar although the tests only exercised the CMOS.

This integration process is not limited to the single-level polysilicon process described here. This process can be used with more intricate micromechanical processes such as the three-level polysilicon technology previously developed at Sandia [3]. An example of this technology built in a trench is shown in Figure 7.

Conclusions

The manufacturability of a technology that integrates surface-micromachined polysilicon structures with microelectronics in a modular fashion has been demonstrated. This technology does not impose additional limits on the size, thickness, or number of layers of the micromechanical polysilicon structures. The modularity of the process allows changes to be made to either the micromechanical process or the microelectronic process without affecting the other process. A planarized wafer with the embedded MEMS can serve as starting material for a conventional microelectronics foundry service since the technology does not require significant modifications of standard microelectronic fabrication processes.

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The process development engineers, operators, and technicians of the Microelectronics Development Laboratory should also be acknowledged for their contributions to the process development, fabrication, and testing of these devices. The authors are particularly indebted to Dale Hetherington for CMP development, Chris Apblett for high-aspect-ratio oxide fill development, Tony Farino for photolithography development, and Bob Timon for wet process development. This work, performed at Sandia National Laboratories, was supported by the U.S. Department of Energy under contract DE-AC04-94AL85000.

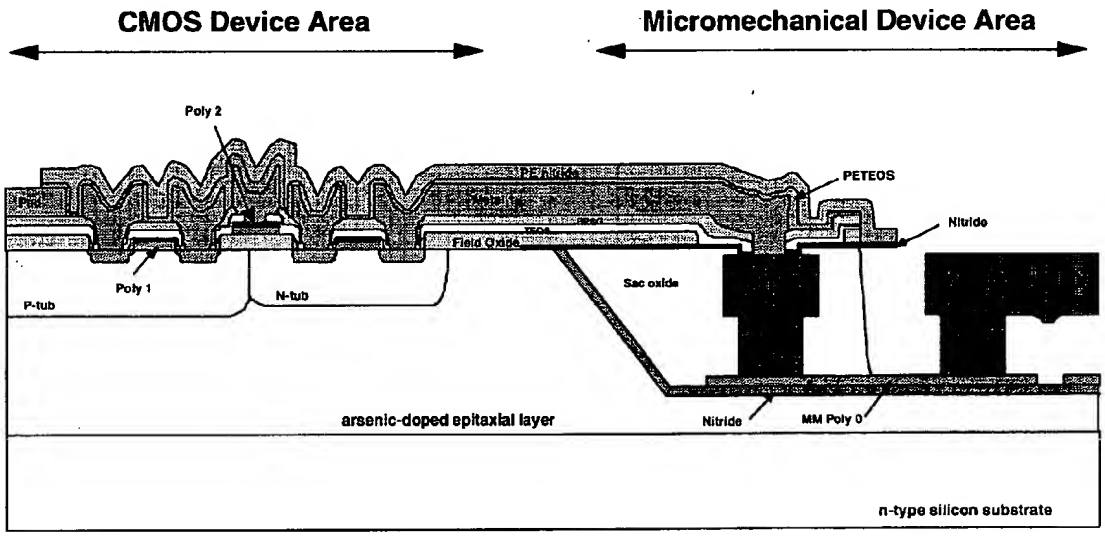

Figure 1. A cross-sectional schematic of the subsurface, embedded MEMS integrated technology.

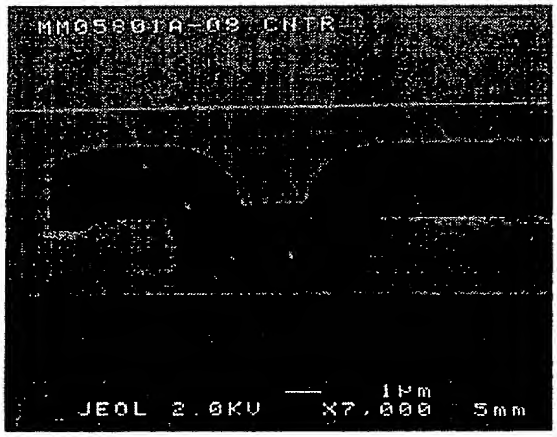

Figure 2. A cross-sectional view of a single-layer polysilicon (with ground plane) structure in a trench. The trench has been refilled with oxide and planarized using chemical-mechanical polishing. This planar structure is ready for standard CMOS processing.

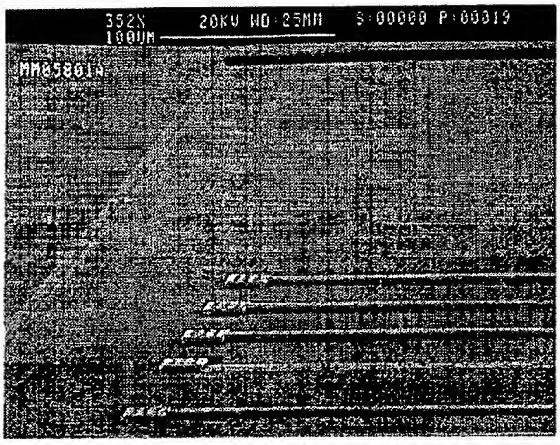

Figure 3. Interconnects leading to polysilicon studs for contact to CMOS metallization prior to fabrication of electronics.

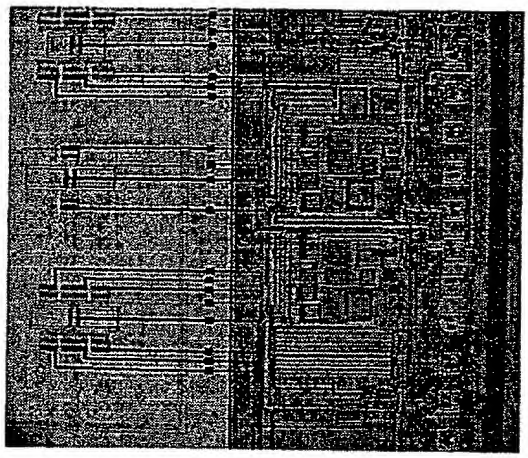

Figure 4. Surface-micromachined polysilicon resonators built in a trench alongside their CMOS sensing electronics. The marks on the bonding pads were caused during wafer-level testing.

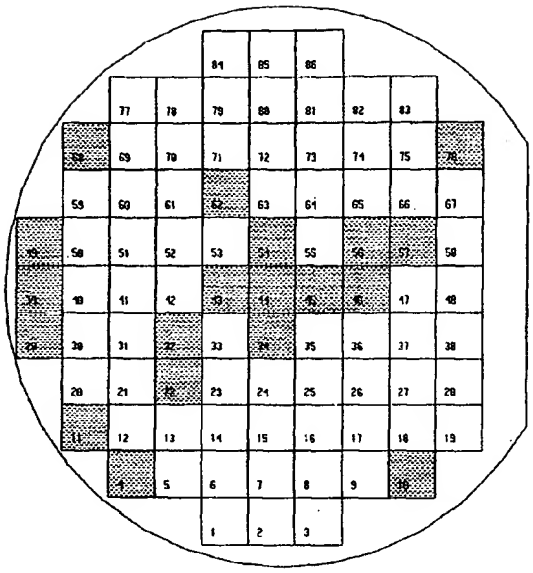

Figure 6. A wafer map showing functionality from a wafer-level test of combustible gas sensor devices. The unshaded devices are functional.

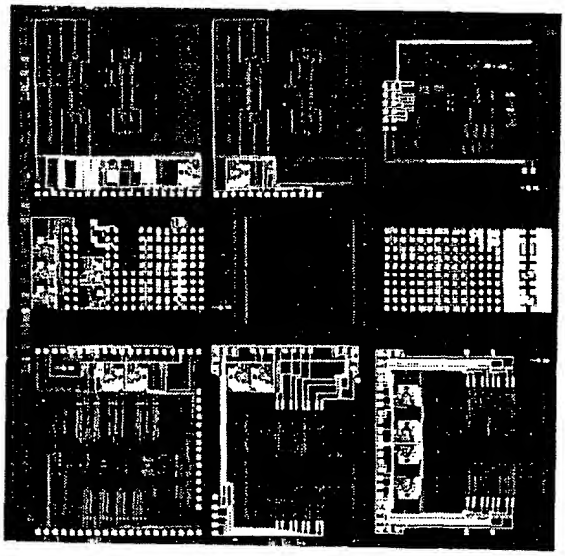

Figure 5. An photograph of the completed integrated MEMS/CMOS die illustrating the layout of the various sensors, resonators, test structures, and electronics.

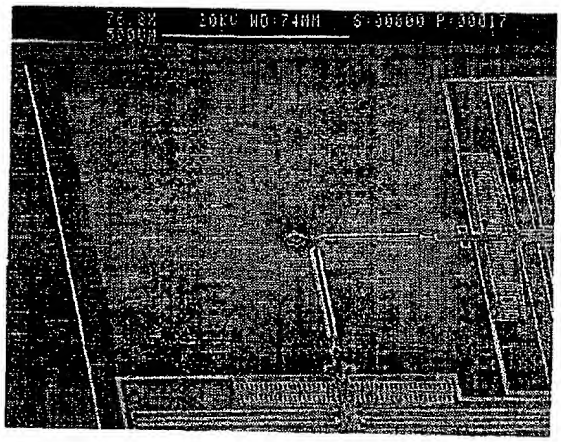

Figure 7. A three-level polysilicon structure (microengine) built in a trench. Here, the trench depth is approximately 12 μm.

POLYSILICON INTEGRATED MICROSYSTEMS: TECHNOLOGIES AND APPLICATIONS

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ABSTRACT

Merging polysilicon microstructures with CMOS electronics offers monolithic solutions for inertial sensing and micromechanical signal processing. Correlations between polysilicon deposition, doping, and anneal conditions and the mechanical properties are understood. A low-thermal-impact polysilicon process could be merged with submicron CMOS. In vacuum, the Brownian noise of a polysilicon accelerometer is about 1 $\mu g/Hz^{1/2}$. An integrated sigma-delta controller, implemented in 1 μm CMOS, can in principle resolve this noise. Microresonator oscillators and filters are of potential application in low-power electronic signal processing. Building-block approaches to microsystem design are emerging.

INTRODUCTION

Polysilicon surface microstructures were first reported in 1982 [1], followed shortly by the initial demonstration of an integrated NMOS/polysilicon process in 1984 [2]. Integrated electronics were necessary for detecting the very small motional current from the microresonator. It was also assumed that increased levels of functional integration was the natural direction for technology evolution.

Over the past decade, polysilicon integrated microsystems have been successfully commercialized, with introduction of a 50 g air-bag accelerometer in 1993 [3] and a 5 g accelerometer at this conference by Analog Devices, Inc. [4]. The potential applications of this integrated technology (BiMOS2E) are being explored by academic researchers at BSAC and other US institutions [5]. Initial results are very encouraging that the "application space" of this technology includes a wide range of inertial sensors and microresonators.

This paper provides an overview and perspective on polysilicon integrated microsystems, beginning with polysilicon as a microstructural material. The thermal cycles and topography of CMOS and polysilicon microstructures determine the strategies for developing a merged technology. Building blocks for suspensions, position sensing, and electrostatic actuation are described in the context of a closed-loop, digital output accelerometer and a microresonant structure. Brownian motion is relatively large in polysilicon surface microstructures, since their mass is on the order of 10^{-9} kg, or less. Sigma-delta approaches to closed-loop control of sense elements are important for surface microstructures, since they relax the requirements for mechanical symmetry and matching. Due to the rather coarse control of polysilicon linewidth and thickness given by IC technology, trimming is essential to achieve reproducible characteristics. Finally, polysilicon microstructures are not the sole option for integrated microsystems; the paper concludes with an assessment of the several monolithic technologies.

POLYSILICON MICROSTRUCTURES

Polysilicon as a mechanical material has been the subject of extensive study over the past decade. Residual strain and its gradient through the thickness of the film are critical constraints on microstructure design. If the average strain is compressive, then microbridges will buckle, beyond a certain critical length. Strain gradients generate an internal bending moment that causes cantilever beams to warp out-of-plane upon release.

Undoped, fine-grained (or microcrystalline) polysilicon can yield a controlled tensile strain with low-temperature annealing [6]. Conducting polysilicon is very convenient for capacitive position sensing and electrostatic actuation. Earlier work at Berkeley focused on the post-deposition doping and stress anneal of polysilicon films by diffusion of phosphorus from surrounding phosphosilicate glass (PSG) layers, at temperatures of 1050 °C [7]. This polysilicon has a moderate compressive strain and a low strain gradient. Ion-implantation of undoped polysilicon, followed by a furnace anneal, is the structural polysilicon process used in the BiMOS2E integrated technology. This polysilicon has a moderate tensile strain, with a strain gradient that causes cantilevers to deflect toward the substrate [8].

A low-thermal impact conducting polysilicon process is attractive for integrated MEMS. *In situ* doped polysilicon has the advantage of not requiring a high-temperature dopant drive-in step [9]. The lower deposition rate of *in situ* phosphorus-doped polysilicon can be mitigated by reducing the flow of phosphine/silane ratio by one-third. Deposition at 585 °C (for a 2 μm-thick film), followed by 900 °C rapid-thermal annealing (RTA) for 7 minutes, results in a polysilicon film with low residual tensile strain, negligible strain gradient, and low resistivity [10,11].

The release of polysilicon microstructures involves extended etching of the underlying sacrificial oxide layer in hydrofluoric acid [12]. Adhesion of polysilicon microstructures to the substrate can occur after surface-tension-induced collapse during drying after the final rinse. Several approaches to "stiction-free" drying have been demon-

strated [13-15]. However, the post-release stiction of microstructures remains a concern. Given a sufficient impulse, microstructures will deflect and contact adjacent surfaces. Self-assembled monolayer organic coatings [16], diamond-like carbon coatings [17], and a simple hydrogen-termination process [18] all result in low-adhesion surfaces on polysilicon microstructures.

INTEGRATED PROCESSES

In evaluating the co-fabrication of polysilicon microstructures with CMOS, the thermal budget required for the polysilicon process is a primary consideration. Even with the recently developed low-thermal impact polysilicon, the microstructural films must be deposited and annealed prior to any aluminum layers. Another consideration is that the typical step height of the polysilicon/PSG layers in the microstructure is 4-5 μm for a single structural layer and 6-7 μm for two structural layers [9]. The rough topography places severe demands on the lithography and etching processes for subsequent layers. For this reason, along with concerns about contamination, insertion of the microstructure process prior to CMOS has not been attractive.

At BSAC, the modular "MICS" technology has been developed for the post-CMOS fabrication of polysilicon microstructures [9]. In order to raise the temperature ceiling of the CMOS, tungsten is used instead of aluminum for the metallization. $TiSi_2$/TiN diffusion barriers in the contacts prevent WSi_2 formation during RTA at 900 °C for 60 seconds, which is sufficient for the stress anneal of the *in situ* structural polysilicon layers. Hillock formation in the W metal lines during annealing and high contact resistance remain problems in the MICS process [9]. The former problem can lead to failure of the Si_3N_4 passivation layer protecting the CMOS during the HF release etch, necessitating a photoresist release mask.

Although not a completely modular solution, the process flow in Fig. 1 is an attractive strategy for polysilicon integrated microsystems. The micromachining sequence is inserted after completion of the electronic structures, but prior to contact etching or aluminum metallization, which is the basic strategy used in earlier work [2,8,19]. The low-phosphorus *in situ* polysilicon process requires 7 minute anneal at 900 °C, or less if some strain gradient can be tolerated [10,11]. Since a source/drain anneal for a sub-μm technology is on the order of 30 minutes at 900 °C, the polysilicon anneal causes only minor dopant redistribution in a typical CMOS process. The contact and metallization lithography and etching steps will require process modifications, due to the "islands" of severe topography created by the thin-film stacks of PSG and structural polysilicon.

In Fig. 1, the CMOS area is protected with Si_3N_4 prior to microstructure fabrication. Contacts are made to gate or capacitor polysilicon prior to deposition of the polysilicon bottom electrode layer [9], in order to interconnect the CMOS circuitry with the microstructure. After deposition and patterning of the microstructural films, the microstructure area is passivated and the CMOS is exposed to proceed with aluminum metallization. During the sacrificial layer etching in HF, the circuit area is protected by a photoresist release mask [2,8], after which the structure is dried, preferably using one of the stiction-free techniques. The bonding pads must also be exposed after release, except where an HF-resistant metal such as gold is used [19]. At some point during or after the release process, the polysilicon surfaces can be treated to reduce "in-use' stiction.

The mask count for a polysilicon microsystem process is about 7-10 over that of the CMOS process, for a total of about 15-20. As will be seen, there is no need for "state-of-the-art" sub-micron lithography and etching for either the electronic or the microstructure modules and consequently, the yield of the overall process can be high. Polysilicon microsystems are basically ICs with added non-electrical measurement capability -- the fractional area consumed by the polysilicon microstructures is small [8,20].

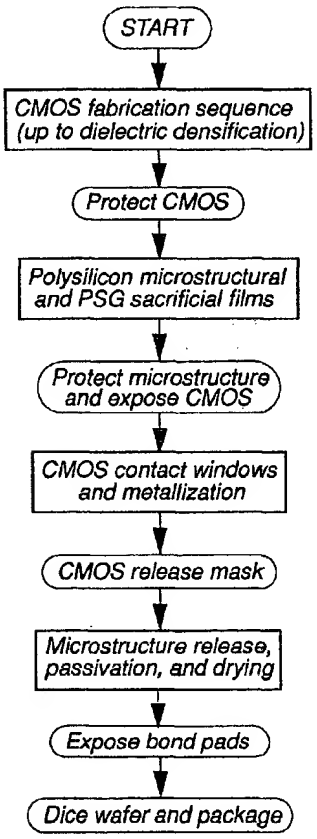

Figure 1 Polysilicon microsystem process flow.

POLYSILICON MEMS BUILDING BLOCKS

Polysilicon is an excellent material for suspensions, due to its low density and high mechanical quality factor of about 50,000 in vacuum. Beam widths of 1.5 μm are feasible in 2 μm-thick structural polysilicon using optical lithography and reactive-ion-etching. By using sidewall structures [21], much higher aspect ratio (thickness-to-

width) polysilicon beams are possible. In order to eliminate the effect of compressive or tensile residual strain on the spring rate, folded [7,21] or meander [22] suspensions are desirable. However, these suspensions are more susceptible than clamped tethers [8] to residual strain gradients. The variations in width and thickness of a polysilicon suspension are both on the order of 10%, from lot to lot. Without considering material property variations [8,10,11], some means of trimming the spring rate is necessary for precision applications [22,23].

Examples of capacitive position sensing structures are interdigitated combs for in-plane displacements [3] and parallel-plates for movement normal to the substrate [20]. These same structures can also be used as electrostatic actuators. For in-plane displacements, symmetrical comb sense capacitors and electrostatic comb feedback actuators are used in analog accelerometers [3,4]. The versatile comb structure can be also used to levitate a microstructure, as shown in the accelerometer below [20].

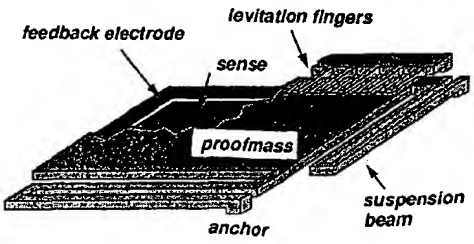

Figure 2 Schematic of z-axis accelerometer, showing 2 of the 4 suspension beams and a segment of levitation fingers, which extend around the perimeter of the proof mass [20].

The asymmetrical sense element in Fig. 2 is representative of surface microstructures that sense out-of-plane motion. Even with a second polysilicon structural layer [9], a well-matched differential sense capacitor cannot be achieved. A closed-loop accelerometer using the sense element in Fig. 2 has been demonstrated [20] by applying a DC voltage V to the interdigitated comb to generate a constant levitation. The underlying feedback electrode supplies the variable balancing force.

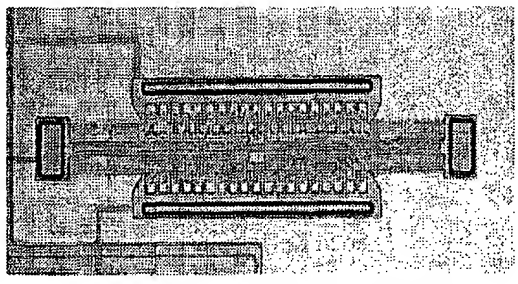

Figure 3 Comb-driven double-ended tuning fork.

Electrostatic comb drives apply a force that is independent of displacement, to first order [7]. This property makes them desirable for microresonator drive and detection, as shown in the double-ended tuning fork example in Fig. 3. Micromechanical resonators have potential applications in integrated frequency references and micromechanical filters and mixers, as well as in sensors [24,25].

CMOS INTERFACE/CONTROL CIRCUITS

Brownian motion is the fundamental position noise for polysilicon surface microstructures, due to their low mass. In vacuum, the equivalent Brownian acceleration noise is about 1 $\mu g/Hz^{1/2}$ for a structure with a mass of 5×10^{-10} kg and a resonant frequency of 5 kHz, assuming a quality factor of 50,000, which is equivalent to a position noise of 10^{-4} $Å/Hz^{1/2}$ [26]. The capacitive sense circuit must resolve the Brownian motion, in order not to limit the sensor performance. For both a unity-gain buffer and an integrating amplifier, this goal can be achieved, in principle, if the CMOS technology has a cutoff frequency on the order of $f_T = 500$ MHz or greater [26].

Given the asymmetries inherent in surface micromachined sense elements, a pulse-modulation feedback scheme is attractive [20,26]. This approach eliminates the need for precise matching of differential capacitors for linearization of the quadratic electrostatic feedback force. In addition, the requirements on the CMOS interface circuit are relaxed. A one-bit decision is made on the proof mass position every clock cycle; the output of the sensor is a digital bit stream at the sampling frequency. This control loop is equivalent to the sigma-delta modulator used in analog-to-digital conversion and is especially well-suited to low-bandwidth inertial sensors. As the sampling frequency is increased, the various artifacts of the quantization process, such as the dead zone width, are reduced [26]. A die photo of a monolithic digital force-feedback accelerometer, with functional blocks identified, is shown in Fig. 4.

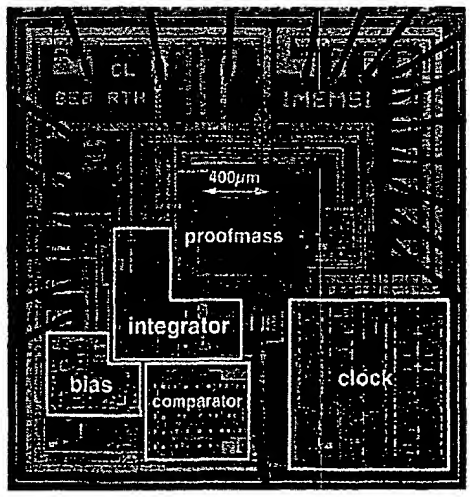

Figure 4 Monolithic z-axis accelerometer with sense element illustrated in Fig. 2, fabricated in BiMOS2E [20].

Microresonant structures require a transimpedance amplifier to detect the motional current from sense electrode, which can be easily implemented in CMOS [24]. In order to satisfy the phase condition for self-oscillation, the phase shift through the amplifier should be 0^o or 180^oC. MOS transistors biased in the linear region are useful for implementing the large on-chip resistance [25].

CONCLUSIONS

Monolithic solutions for inertial sensing are feasible using polysilicon microsystems. The initial designs on the first BiMOS2E multi-project chip run demonstrate that several inertial variables can be measured. A multi-sensing chip would be useful for head-mounted display systems, or for navigation in automated highway systems, to name two applications that are motivating research in BSAC. In order to reach the Brownian noise floor for inertial sensors and to reduce the chip size for multisensors, a denser, higher f_T CMOS process is needed. A new technology currently under development at Analog Devices will combine digital CMOS with enhanced microstructures.

Microsystem design is currently hampered by the lack of generally available integrated CAD tools, although progress is being made [27]. Finally, the micro electromechanical and CMOS building blocks developed for polysilicon microsystems also apply to technologies based on thin-film or plated metal microstructures [28,29], as well as single crystal silicon [30]. The next five years will prove interesting, as the various integrated microsystem technologies are applied to solve real-world problems.

ACKNOWLEDGEMENTS

The author acknowledges the major contributions of his current and former graduate students and J. M. Bustillo, BSAC process engineer. Prof. B. E. Boser has contributed greatly to the design and modeling of integrated microsystems. He is grateful to Drs. R. S. Payne of Analog Devices and K. J. Gabriel of ARPA for supporting microsystems research at BSAC.

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Surface-Micromachined Resonant Accelerometer

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SUMMARY

This paper discusses the design and testing of a resonant accelerometer developed for integrated surface-micromachining processes. First- and second-generation designs are presented. The sensors use leverage mechanisms to transfer force from a proof mass to double-ended tuning fork (DETF) resonators used as force transducers. Each fork forms the basis of an integrated oscillator to provide the output waveforms. The DETFs on the first-generation device have a nominal frequency of 175 kHz, and the sensor has a scale factor of 2.4 Hz/g. The oscillators on this device exhibit a root Allan variance floor of 38 mHz (220 ppb). The second-generation, higher-sensitivity sensor uses DETFs with a nominal frequency of 68 kHz and has a measured scale factor of 45 Hz/g.

Keywords: Surface-micromachining, resonator, accelerometer

INTRODUCTION

A resonant sensor is a device whose response to the measurand is a frequency shift. Historically, sensors based on vibrating elements have been considered highly attractive, as they are generally quite sensitive and possess a wide dynamic range [1]. The quasi-digital nature of the output signal also makes this sensor class easy to integrate into digital systems [2]. Quartz-based resonant sensors have been used in many commercial applications, including navigation-grade precision accelerometers [2][3].

Some recent work has focussed on micromachined resonant sensors in bulk silicon processes [4][5], but this class of sensor has not yet been pursued in a surface-micromachining technology. Because of this, the design trade-offs are not yet well-understood. Resonant sensing is a powerful measurement technique, and surface-micromachining has already proven itself as a manufacturable technology. The combination of the two has the potential to produce high-quality, low-cost sensors.

To demonstrate the feasibility of resonant accelerometers in a surface-micromachining technology, a prototype device has been fabricated at Analog Devices, Inc. in the BiMEMS foundry process. The transducers themselves are double-ended tuning fork (DETF) resonators whose natural frequencies are a function of an applied force. Force is transferred to the forks from the proof mass by a leverage mechanism. This mechanism also amplifies the force during the transfer, increasing the scale factor of the sensor. Oscillators based on the tuning forks provide the output waveforms of the device. A microphotograph of the die, which contains four separate devices and some unrelated stiction experiments, is shown in Figure 1.

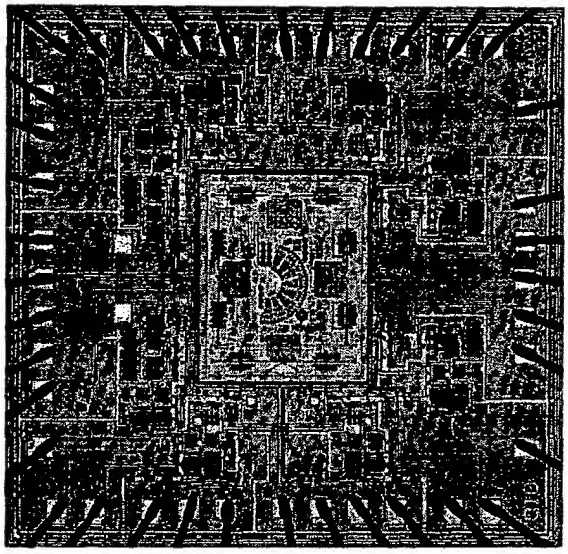

Figure 1: Die photo of ADI-fabricated accelerometer chip

MECHANICAL DESIGN

A microphotograph of the accelerometer itself is shown in Figure 2. The polysilicon is 2 μm thick, the tuning fork tines are 2 μm x 220 μm, and the proof mass is approximately 120 μm x 150 μm. When an acceleration is applied to the device, the proof mass hinges about the pivot beam and applies forces to the two DETFs. One of these forks is subject to a tensile force which raises its natural frequency. The other experiences a compressive force, lowering its frequency. Each fork is kept resonating at its natural frequency by a sustaining amplifier, and the frequency difference between the two forks is the output of the sensor. This push-pull configuration gives the device a first-order temperature compensation.

In order to maximize the scale factor available from the small inertial mass, a leverage system is used to magnify the force applied to the tuning forks [6]. The pivot beam and proof mass approximate a fulcrum and lever, as shown in Figure 3. This magnifies the force applied to the tuning forks by approximately an order of magnitude. Naturally, the scale factor of the sensor is magnified by the same amount. To compensate for any bending moments applied to the tuning forks, the beams linking

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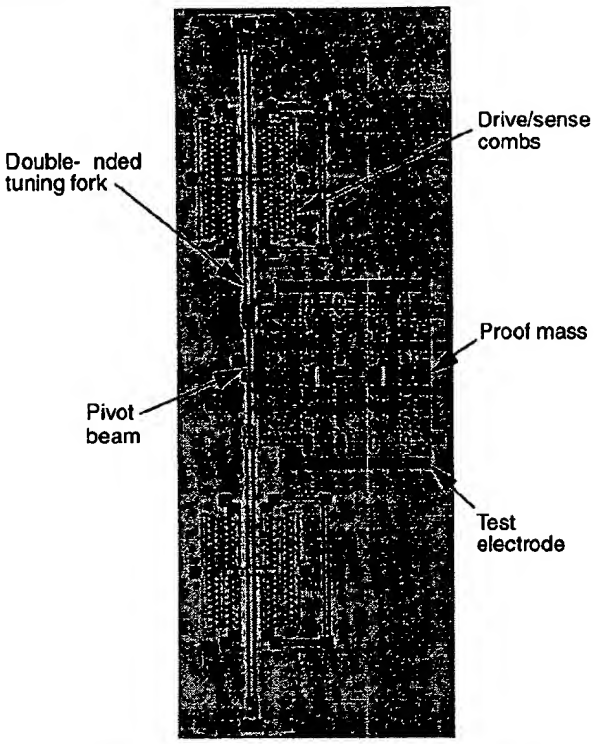

Figure 2: Microphotograph of fabricated accelerometer

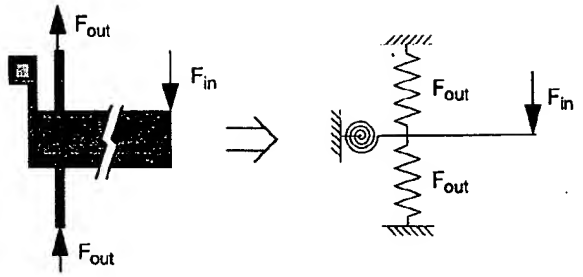

Figure 3: Spring-lever model of leverage mechanism

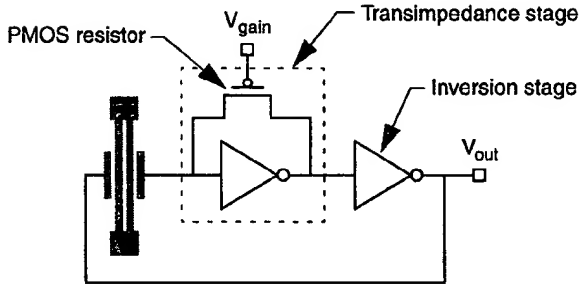

Figure 4: Simplified schematic of oscillation loop

the DETF structure to the lever arm are dimensioned so that the average moment across each tuning fork is zero. This insures that the tuning fork tines are not differentially loaded [6].

ELECTRICAL DESIGN

Each of the tuning forks on the accelerometer structure has its own sustaining amplifier. In each case, the amplifier and tuning fork form an oscillation loop that generates an output waveform at the natural frequency of the DETF. These oscillators must be as stable as possible in order to minimize the sensor noise floor.

The oscillation loop is shown in Figure 4. The tuning fork itself is a variant of previously-demonstrated micromachined resonators [7]. Each tine has drive and sense combs attached to it, and the two tines of each fork are driven and sensed in parallel. This arrangement rejects unwanted vibration modes and gives the resonator a series RLC electrical model similar to that of a quartz crystal. Near resonance, the reactive component of the impedance is small, and the DETF has a primarily resistive behavior.

The amplifier, whose purpose is to convert the output current from the tuning fork into a voltage used to drive the structure, consists of two inverter stages [7]. The first stage is an inverting amplifier with a PMOS device used as a resistor placed in feedback around it. This stage is responsible for the actual transimpedance function, with the PMOS device serving as a variable resistor that sets the gain of the stage. The second stage is a simple inverting amplifier, the output of which is sent both to an output buffer and back to the fork itself.

Left to itself, this circuit would drive its tuning fork far into the nonlinear vibration regime, which is detrimental to oscillator stability [8]. To limit the amplitude of oscillation, an off-chip gain control loop was implemented. After filtering, a diode rectifier and low pass filter are used to detect the output amplitude and set the voltage on the gate of the PMOS resistor. The effect is that as the oscillation amplitude grows, the gain of the amplifier drops. When the gain is no longer enough to cause the amplitude to increase further, a steady state condition is reached.

FABRICATION AND TESTING

The resonant accelerometer described above was fabricated in the Analog Devices BiMEMS foundry process [9]. In order to achieve a sufficiently high Q for oscillation, the device had to be tested in vacuum. A bell jar was constructed to allow a ceramic DIP package to be held at 150 mTorr by a roughing pump during testing. The feedthroughs of this bell jar were attached to a circuit board, and the board and jar were bolted together. This allowed gravitational acceleration to be applied to the chip while in vacuum. For higher forces, the test electrodes to either side of the proof mass were used to apply electrostatic forces.

The response of the individual tuning forks to these applied forces is shown in Figure 5. The nominal frequencies of the

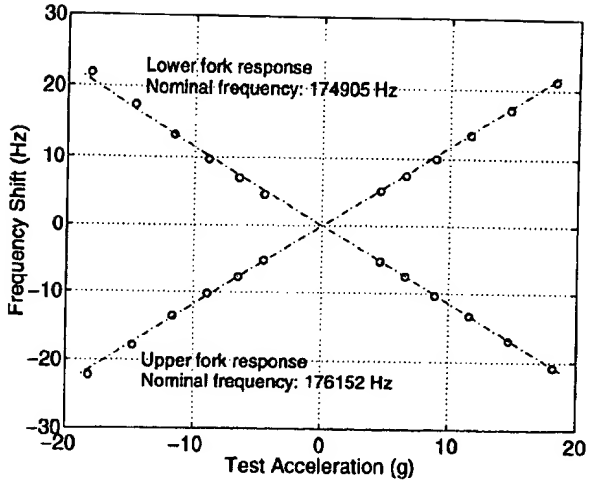

Figure 5: Tuning fork response to applied forces

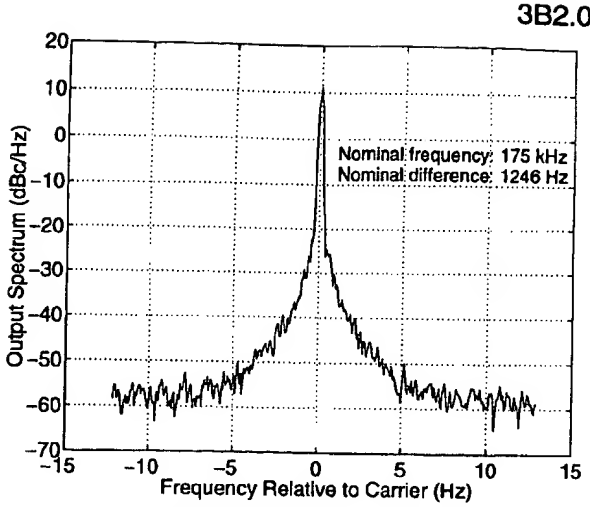

Figure 6: Frequency difference output spectrum

forks are 174.9 and 176.1 kHz, a mismatch of 0.7%. The scale factor as measured with a ±1g test is 2.4 Hz/g. As can be seen, the response of each fork is in line with expectations, and the sensitivities of the two forks are well-matched, despite the asymmetry of the sensor design.

In order to characterize the oscillators, the two outputs were multiplied against each other, the high-frequency component was removed, and the resulting frequency difference was analyzed. The noise contributions from each fork were assumed to be equal, an assumption borne out by comparison of the two power spectra. This analysis method allowed the measurement of small fractional fluctuations without need of an external reference. The Allan variance was chosen as a figure of merit based on its applicability to signal processing of resonant sensor outputs [4].

The frequency difference power spectrum and single-oscillator Allan variance data are shown in Figures 6 and 7, respectively. For an oscillation amplitude such that the noise floor is 58 dB/Hz below the carrier, the constant region of the root Allan variance, or "frequency flicker floor," occurs at 38 mHz (220 ppb). Using model fitting techniques, the Q of open-loop forks on the same chip was estimated at 72,000.

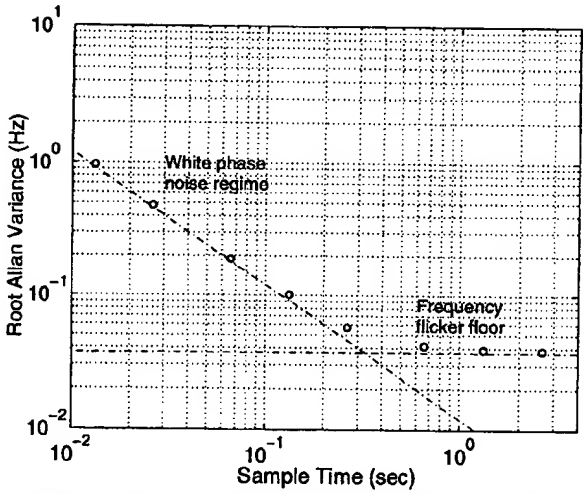

Figure 7: Allan variance behavior of integrated oscillator

DISCUSSION

Much better noise performance can be expected from oscillators based on these high-Q elements. There are two major sources of noise present in this system, one linear and one nonlinear. The dominant linear noise source is the PMOS resistor in the sustaining amplifier. This resistor, located at the front end of the circuit, generates a large amount of current noise and gives the oscillation loop a very high noise floor. The effect at low oscillation amplitudes is to bury the signal in white noise, making it hard to detect and difficult to limit to linear regimes of operation. If the noise due to this source demands that the oscillation be at a nonlinear amplitude, the oscillator will never be very stable. In addition, this noise source is responsible for the $1/\tau$ portion of the root Allan variance graph, demonstrating that white noise hinders frequency measurements at high rates. An improved front end of this circuit based on a Pierce configuration [10] should reduce this noise source by at least an order of magnitude.

The second noise source in this system is nonlinear and the dominant noise source at lower sampling frequencies. This source has been shown to be a nonlinear mixing of the 1/f noise of the sustaining amplifier around the carrier signal [8]. This mixing takes place when low-frequency drift in the sustaining circuits causes a series resistance drift in the tuning fork itself. Because the resonator is not vibrating in a truly linear regime, some amplitude-frequency effect remains. The resistance shift interacts with the gain control circuitry to produce an amplitude shift and along with it, a change in frequency. This noise source is responsible for the flicker floor, beyond which further time-averaging produces no decrease in frequency fluctuation. It can be minimized by reducing the amplitude of vibration to reduce

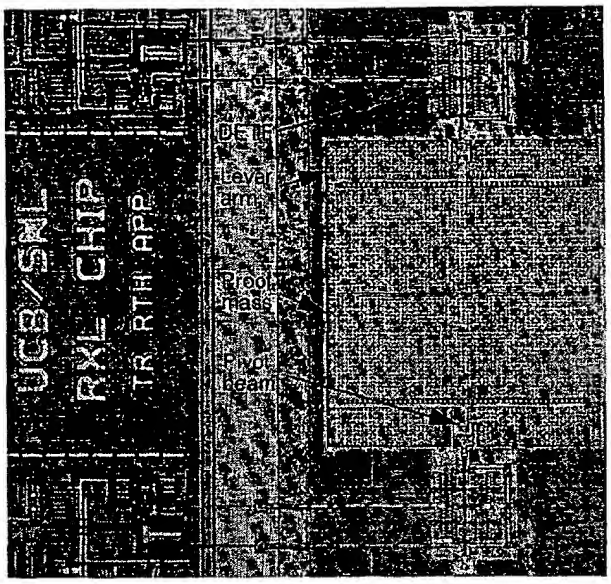

Figure 8: Photograph of second-generation accelerometer

the nonlinearity, by reducing the 1/f noise of the circuitry, or by an integrated AC-coupling scheme to remove the low-frequency drift from the tuning fork drive comb.

The two primary factors affecting the noise floor of a resonant sensor are the scale factor of the device and stability of its oscillators. While the first-generation design is useful to show proof of concept, it does not maximize the scale factor possible in a surface micromachining technology. To this end, a second-generation accelerometer, shown in Figure 8, has been fabricated in the integrated surface-micromachining process at Sandia National Labs [11]. The polysilicon is 2 μm thick, the DETFs are 2 μm x 180 μm, and the proof mass is approximately 460 μm x 540 μm.

The mechanical design of this sensor incorporates several design improvements. The low-stress-gradient polysilicon allows a larger proof mass, and the improved leverage system provides greater magnification, both of which increase the scale factor. Making the leverage system symmetric removes any potential sensitivity to angular accelerations and improves the overall robustness of the device. It also removes the necessity of designing the tuning fork against transferred moments. Testing on the device is still underway, but in initial characterization, the sensor has shown a base output frequency of 68 kHz and has demonstrated a sensitivity of 45 Hz/g in ±1g tests.

CONCLUSIONS

First- and second-generation resonant accelerometer designs have been produced in two different surface-micromachining technologies. These devices are functional and their behavior is in line with expectations. With the further study of these sensors and their design models, the trade-offs involved in using resonant sensing techniques in surface-micromachining technologies can be more deeply understood. Future work will include design of lower-noise oscillators and testing of shock and temperature sensitivities.

ACKNOWLEDGEMENTS

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Batch Transfer of Microstructures using Flip-Chip Solder Bump Bonding

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SUMMARY

This paper describes a novel method for transfer and assembly of microstructures using sacrificial-layer micromachining and flip-chip bonding. The technique is performed at room temperature (cold weld) and at the back end of the process flow, and may thus provide a commercially viable alternative to monolithic integration and costly hybrid packages. The transfer is achieved using break-away tethers and by cold welding electroplated indium solder bumps to thick electroplated copper pads. Both high aspect ratio MEMS devices as well as surface micromachined devices have been successfully transferred using this method with no observable misalignment between moving and stationary parts. The ultimate tensile and shear strength of the solder bond is measured to be 11±3 MPa and 9±1 MPa respectively. The contact resistance is measured to be of the order of 1.5 mΩ for a 65 μm x 65 μm x 4 μm indium bump.

Keywords: Flip-chip, microassembly, solder-bonding.

INTRODUCTION

A perennial problem in MEMS has been to integrate emerging sensor and actuator processes with existing electronics and packaging technology. Flip-chip bonding, first introduced in the 1960's, has been used to connect IC chips to printed circuits and substrate carriers. Recently, flip-chip has also been used to bond MEMS chiplets to electronics [1]. This paper describes a modified flip-chip method for the transfer of released microstructures. Previous work [2] focused on packaging applications, whereas transfer of functioning, released microactuators and resonators is now described. This technique differs from other structure-transfer methods [3] by virtue of being a thin-film process. The method of integration described in this paper will eventually enable bonding of microstructures onto an IC with peripheral or even underlying electronics. The shortened signal path will improve operating speed and signal-to-noise ratio. Two types of structures have been transferred, surface-micromachined resonators and rotary microactuators [4] fabricated using the HexSil process [5]. Since the integration is performed as the last step, this approach allows electronics and MEMS to be produced separately, thereby simplifying fabrication.

PROCESS DESCRIPTION

Figure 1 shows the process flow for microstructure transfer. This process is suitable for wafer to wafer transfers but this work focuses on chip level transfers for initial process development. The polysilicon MEMS structure is first fabricated. The

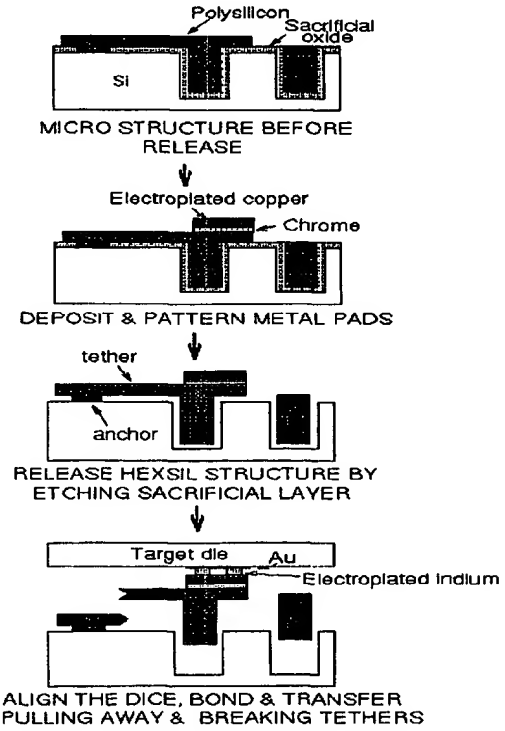

Figure 1. Microstructure transfer process.

first structure used for this study is a two-piece HexSil electrostatic actuator. Thick copper pads (5 to 8 μm) are then electroplated in the regions to be bonded (shown in Figure 2(a)). A chrome-copper seed layer is used. The microstructures are then released by etching away an underlying sacrificial oxide layer using concentrated HF. No significant attack of the metallization is observed in the course of a 3 to 10 minute release. After release, the structures are held in place by polysilicon tethers patterned on the surface. A target die (in this case a glass substrate) is patterned with metal bond pads. Indium bumps (50 μm in diameter and 15 μm thick, as shown in Figure 2(b)), are then plated onto the bond pads. The copper pads on the MEMS die are then aligned with the bumps on the target die. The dice are cleaned with 10:1 HCl just prior to alignment. Cleanliness of the metal surfaces is important for a good bond. Once aligned the two dice are pressed together and bonded by cold welding the indium solder to the copper. It is observed that sufficient contact pressures yield good bonds without the need for solder reflow. The recommended pressure for cold welding is 350 MPa but structures have been transferred using much lower pressures (~ 20 MPa). Alternatively, a reflow at 170 °C for 30 sec can be employed if the structures are

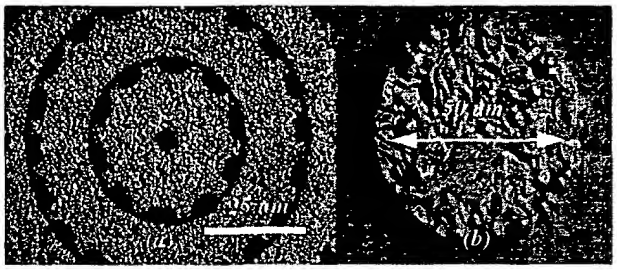

Figure 2. (a). Electroplated copper on polysilicon microstructure. (b). Electroplated indium bump

too fragile to withstand the cold weld contact pressure. The use of indium allows fluxless soldering. In the final step the dice are carefully separated, breaking the tethers, and thereby transferring the microstructures onto the substrate. The same process is used to transfer surface micromachined resonators.

RESULTS

Figure 3 & Figure 4 show a 40 µm thick rotary microactuator bonded to a glass substrate. The stator and rotor of the actuator, though anchored separately, displayed no misalignment (down to an observable limit of ~0.25 µm). The performance of these transferred microactuators is described in [4]. Polysilicon sur-

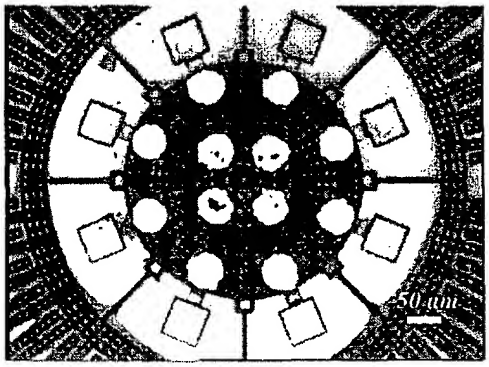

Figure 3. Bottom view through the glass substrate of actuator bonded via indium bumps.

face micromachined resonators are also transferred to a glass substrate using the indium solder bump process. Fabrication process flow is the same as for the HexSil actuators, with the omission of the bulk etch step. The resonators are designed to oscillate both horizontally and vertically, for possible use in pressure sensing or characterization of vacuum micro-packages. Figure 5 shows a microresonator transferred from a silicon wafer onto a glass substrate using indium, cold welded at a pressure of 350 MPa. Light areas on substrate are 1 µm plated copper for solder metallization and interconnect. Beams are 500 µm x 8 µm wide. Figure 6 is a close-up of the comb teeth demonstrating vertical and horizontal alignment. As may be seen in the figures, the process is capable of maintaining high dimensional accuracy among transferred parts. As in the case of the actuators, no misalignment of the resonator comb structures

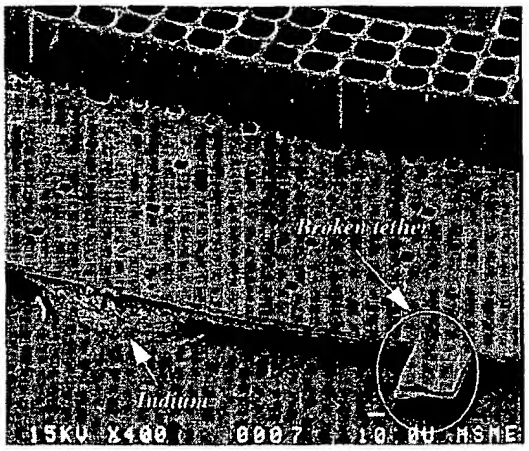

Figure 4. SEM of a microactuator bond pad after reflow of the indium bump.

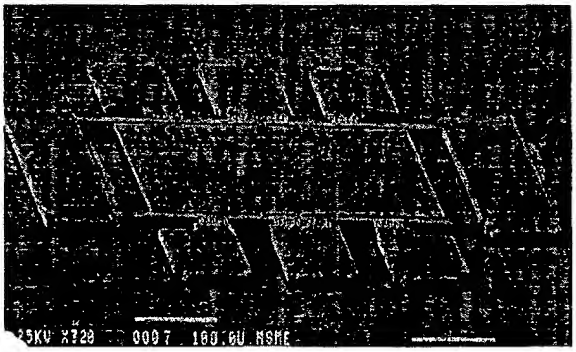

Figure 5. Microresonator transferred onto glass using cold-weld bond.

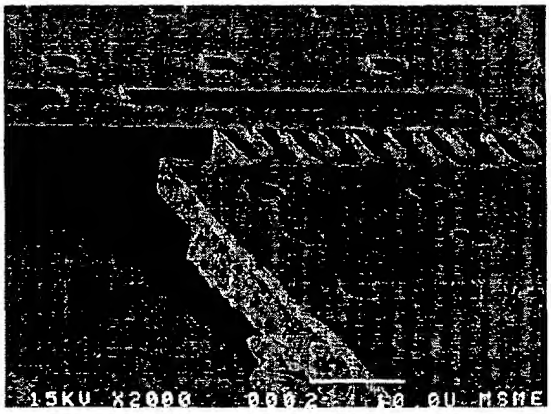

Figure 6. Detail of transferred resonator showing alignment of comb structures.

is evident in the SEM images. Additionally, a simple model [6] predicts that a relative misalignment of as little as 0.1 µm would buckle the resonator beams, with a resulting vertical displacement of more than 2 µm at the center. Buckling was, in fact, observed, until the press apparatus was modified to provide more lateral stiffness. 100% transfer of intact structures is now observed in most samples. Each sample consisted of a 10 mm

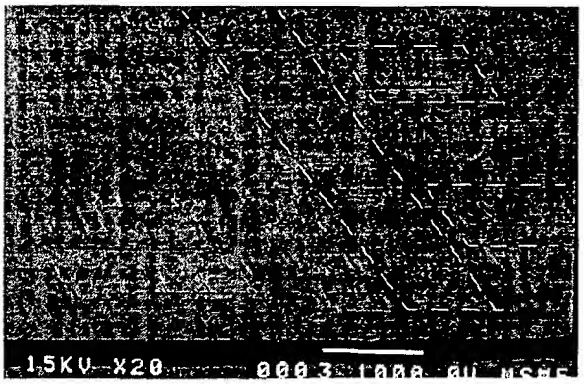

Figure 7. A chip with 12 transferred resonators.

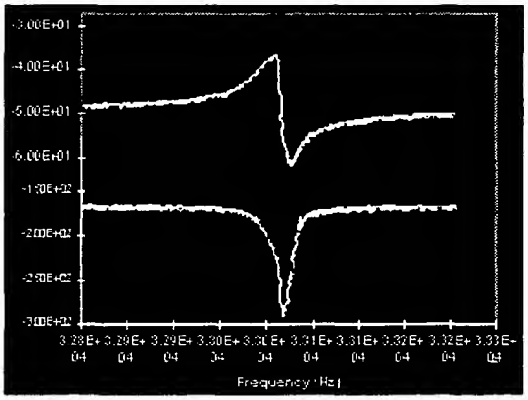

Figure 8. Frequency response of a transferred resonator.

square chip with 12 resonators, and a total of 96 indium bumps. An example is shown in Figure 7. The frequency response of a sample resonator is shown in Figure 8. The asymmetric amplitude curve is due to capacitive feedthrough, which is 180° out of phase with the resonator output. The resonant frequency fo ≡ 33 kHz, which is within 20% of the design. The Q is estimated at about 1,400 at a pressure of 1.5 x 10^{-4} Torr, based on the width of the resonance peak.

Contact resistance

To measure the electrical resistance of the indium to copper cold weld bond, a chain resistor consisting of 32 65 μm square indium bumps (4 μm high) is fabricated by cold welding 2 metallized chips using a contact pressure of 255 MPa. A four point probe setup is used to force current through the resistor and to measure the voltage drop across the 32 bonds. This is illustrated in Figure 9. Since electroplated copper was used to connect the bumps, copper resistors were also fabricated close to the indium-copper chain resistor to accurately estimate the resistance due to copper alone. This is subtracted from the total resistance of the chain resistor to get the resistance due to the bumps only. The contact resistance is measured to be 1.5 mΩ per bump. Since the indium thickness after bonding could not be measured, this roughly translates (based on the plated indium thickness) into a resistivity of 200 - 400 μΩ-cm as compared to 8.4 μΩ-cm for bulk indium. This difference may be due to

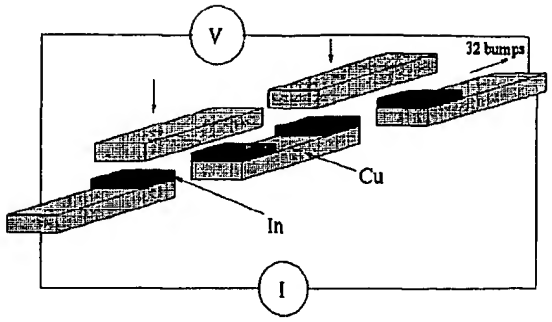

Figure 9. Contact resistance measurement.

native oxide as well other impurities at the indium-copper interface causing a non-uniform bond. Nevertheless, the contact resistance is low enough for many MEMS applications.

Bond strength

The tensile and shear strengths of indium bump bonds are tested using a tensile testing machine. The test chip consists of an array of 2800 bumps, each 65 μm in diameter and spaced 35 μm apart. This chip is pressed into contact with a target chip which has been metallized with 5 μm of electroplated copper. A cold weld is achieved by applying approximately 210 MPa to the chip pair. Once cold welded, the chips are mounted to metal fixtures using an epoxy on the back side of each chip. A separate fixture is used for both tensile and shear testing, as shown in Figure 10. The test results show that the ultimate tensile

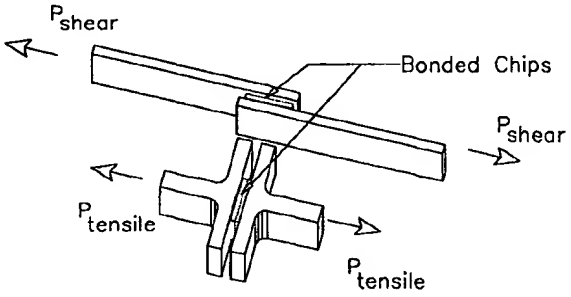

Figure 10. Fixtures used for testing the mechanical properties of Indium solder joints. The top figure is used to test the shear strength of the bumps, while the bottom is used to test the tensile strength.

strength achieved with the bond is 11±3 MPa, while the ultimate shear strength is 9±1 MPa. A typical shear strength test result is shown in Figure 11. Note that the x-axis corresponds to the displacement of the tensile testing frame, not the actual strain on the solder joint. The difference between the properties of bulk indium, which has a yield strength of approximately 2.6 MPa, and those of the electroplated indium solder joints may be accounted for by the fine grain structure of the electroplated metal, as well as the presence of impurities such as indium oxide.

CONCLUSIONS

Successful batch transfer of functioning high aspect ratio

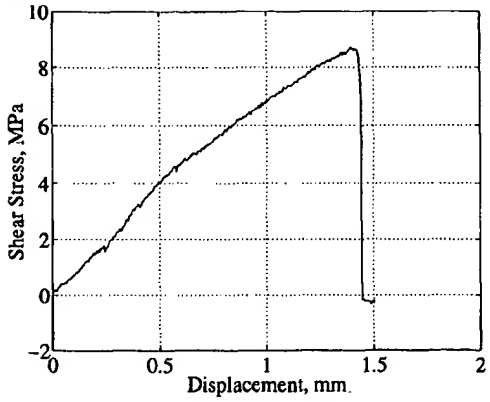

Figure 11. A typical shear testing result. The x-axis is the recorded displacement of the tensile testing frame and is not an accurate measurement of the actual solder bump strain.

microactuators and surface micromachined resonators using flip-chip solder bonding has been achieved. The transfer method using indium solder is relatively simple and with good yield (100% in most cases) and no observable misalignment for both bulk and surface micromachined devices. Ultimate tensile and shear strengths of the solder bond is measured to be 11±3 MPa and 9±1 MPa respectively. The contact resistance is estimated at 1.5 mΩ for a 65 μm square, 4 μm high indium bump. This method of transfer and assembly of microstructures, using break-away tethers and appropriate solders, represents a step towards process "disintegration" wherein MEMS and electronics are fabricated separately and then integrated at the back end of the process flow. Integration of MEMS structures with standard CMOS at minimal additional process cost and complexity may be feasible. Additionally, this technique is intended to operate on the wafer scale, transferring millions of devices per cycle.

FUTURE WORK

Work is in progress to bond MEMS structures onto CMOS chips with underlying electronics. As an alternative to solder-type bonding for MEMS assembly, a solderless, mechanically latching structures is also being developed to allow transfer and temporary attachment of microstructures. This would be followed by vacuum deposition of a metal or other material for permanent bonding. Advantages would include: possible use of aluminum for VLSI compatibility, avoidance of thick solder structures, improved interconnect pitch flexibility. Almost any metal can be vacuum-deposited, whereas choices for fluxless solders are limited. An initial design is shown in Figure 12, with the fabricated, transferred structure in Figure 13.

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Figure 12. Solderless transfer structure. Plated post on target substrate engages slot in polysilicon microstructure. Post is latched by cantilever beam. Further shearing breaks polysilicon tether. Microstructure is automatically aligned to target structure as a result.

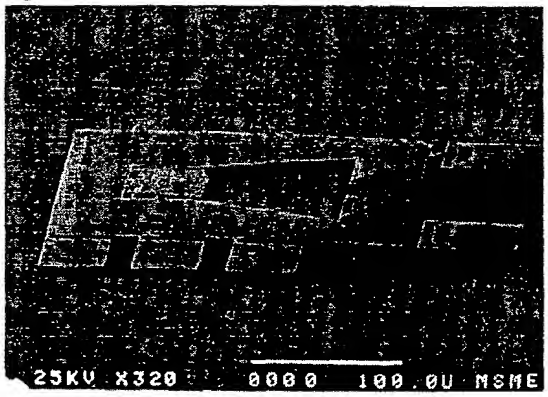

Figure 13. Transferred polysilicon (4 μm thick) latching structure on plated Cu post. The post is 50 μm square and 11 μm high.

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